RC6702

RGB to Y, C_R, C_B Transcoder

Features

- RGB to Y, C_R, C_B matrix, meets CCIR 601-1
- Thin film gain setting resistors
- External gain adjustments pins
- 60 MHz -3 dB bandwidth
- 10 MHz 0.1 dB gain flatness
- 0.06 % differential gain, $R_L \geq 150\ \Omega$
- 0.06° differential phase, $R_L \geq 150\ \Omega$
- 300 V/µS slew rate
- Dual ±5 V power supply
- Low power consumption: 70 mW per amplifier
- 16 pin SO package
- Low offset: 3.0 mV

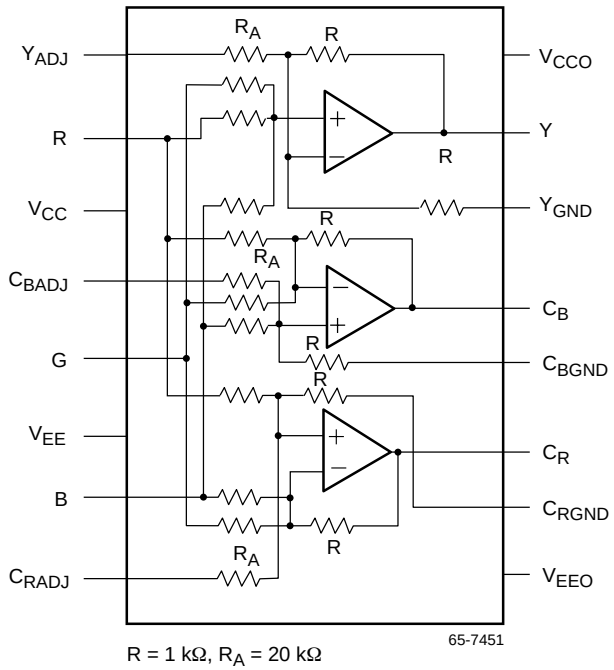
Description

The RC6702 contains three low power, wide bandwidth voltage feedback amplifiers. Internal thin film resistors perform the RGB to Y, C_R, C_B matrixing. The RGB to Y, C_R, C_B matrix is normalized to a gain of two for use in back-terminated video applications. (The sum of the absolute values of R, G and B components in a row is equal to 2.) The matrix gain accuracy is better than 1.0% and the gain temperature drift is below 25 ppm/°C.

Each transcoder has a 60 MHz bandwidth and is flat to ±0.1 dB to 10 MHz. If required, three adjustment inputs allow trimming of the Y gain and C_R, C_B white balance to accuracies better than 0.5%. A 20kΩ potentiometer between +V and -V is required, together with a 50 kΩ series resistor to adjust these offsets (see application circuit).

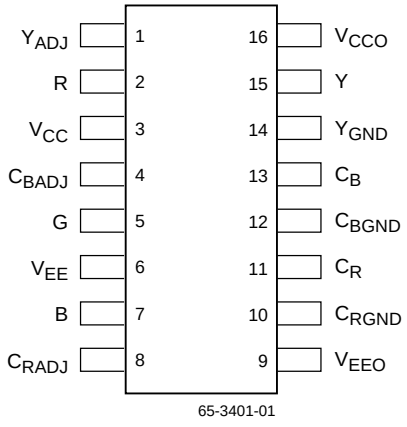
The pinout and layout of the RC6702 minimizes the crosstalk between channels. Each amplifier can drive 35 mA to the load.

Block Diagram



R = 1 kΩ, R_A = 20 kΩ

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
C_{BADJ}	4	C_B Matrix Adjustment Pin
C_{RADJ}	8	C_R Matrix Adjustment Pin
Y_{ADJ}	1	C_R Matrix Adjustment Pin
B	7	B Input
G	5	G Input
R	2	R Input
C_B	13	C_B Output
C_R	11	C_R Output
Y	15	Y Output
V_{CC}	3	+5V Supply
V_{CCO}	16	+5V Output Supply
V_{EE}	6	-5V Supply
V_{EEO}	9	-5V Output Supply
Y_{GND}	14	Y Analog Ground
C_{BGND}	12	C_B Analog Ground
C_{RGND}	10	C_R Analog Ground

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Units
Positive power supply, V_{CC}			7	V
Negative power supply, V_{EE}			-7	V
Differential input voltage			0	V
Operating Temperature	0		+70	°C
Storage Temperature	-40		+125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 seconds)			300	°C
Operating Temperature	0		+70	°C
Short circuit tolerance: No more than one output can be shorted to ground.				

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage	-4.75	-5.0	-5.25	V
θ_{JA}	SO16 Thermal Resistance		105		°C/W

DC Characteristics

V_{CC} = 5V, V_{EE} = -5V, A_V = 2, R_{LOAD} = 150Ω, T_A = 0°C to 70°C, unless otherwise specified. Open Loop.

Parameter		Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	No load		±2	±7	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift[1]			±12		μV/°C
I_B	Input Bias Current [1]			±2	±10	μA
$\Delta I_B/\Delta T$	Input Bias Current Drift[1]			±10	±50	nA/°C
Rin	Input Resistance[1]		1			MΩ
Cin	Input Capacitance[1]			0.5	2	pF
CMIR	Common Mode Input Range		±2.5			V
PSRR	Power Supply Rejection Ratio	No Load	60	70		dB
Is	Quiescent Supply Current	No Load, Whole IC		25	35	mA
R_{OUT}	Output Impedance[1]	Enabled, at DC		0.2		Ω
I_{OUT}	Output Current		35			mA
V_{OUT}	Output Voltage Swing	No load	±2.5	±3.0		V
		R_L=150Ω	±2.5	±3.0		V
Y	White Balance: Gain	R = G = B = 1Vpp	1.97	2.0	2.03	Vpp
C_R, C_B	White Balance, Residual Chroma	R = G = B = 1Vpp	-10	0.0	+10	mVpp
$\Delta A_V/\Delta T$	Closed-loop Gain Drift[1]		25			ppm/°C
Resistor Matrix Characteristics						
A_V	Matrix Gain Accuracy		-1.0		+1.0	%
ΔAv/ΔT	Matrix Gain Drift[1]			20		ppm/°C

Note:

1. Guaranteed by design.

AC Characteristics

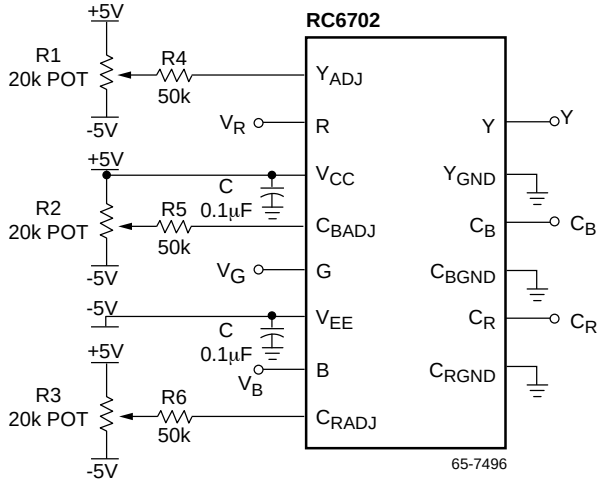
V_{CC} = 5V, V_{EE} = -5V, R_{LOAD} = 150Ω, A_V = 2, T_A = 0 to 70°C, C_L = 10 pF unless otherwise specified.

Parameter		Conditions	Min	Typ	Max	Units
Frequency Response						
BW	-3 dB Bandwidth (A_V = 2)[1]	V_{OUT} = 0.4 Vpp		60		MHz
		V_{OUT} = 0.8 Vpp		55		MHz
Flat	±0.1 dB Bandwidth[1]		10	15		MHz
Peak	Maximum Small Signal AC Peaking[1]			0.4		dB
Time Domain Response						
t_d	Matrix Delay[1]			20		ns
Δt_d	Output's Skew[1]			2		ns
t_{r1}, t_{f1}	Rise and Fall Time 10% to 90%[1]	2V Output Step		7	10	ns
t_S	Settling Time to 0.1 %[1]	2V Output Step		35		ns
OS	Overshoot[1]	2V Output Step		6		%
US	Undershoot[1]	2V Output Step		1.5		%
SR	Slew Rate[1]	V_{OUT} = ±2.0V	200	300		V/µs
Distortion						
HD_2	2nd Harmonic Distortion[1]	V_{OUT} = 0.8 Vpp, @ F_O = 20 MHz		-50		dB
HD_3	3nd Harmonic Distortion [1]	V_{OUT} = 0.8 Vpp, @ F_O = 20 MHz		-50		dB
Equivalent Input Noise						
NF	Noise Floor > 100 KHz[1]			-140		dBm
SND	Spectral Noise Density[1]	100 kHz to 200 MHz		10		nV/√Hz

Note:

1. Guaranteed by design.

Typical Application Circuit



RGB to Y, C_B, C_R matrix, normalized to 2

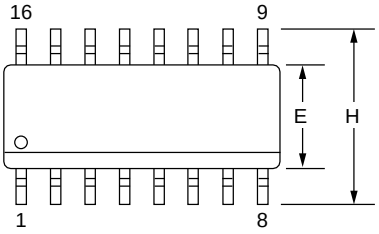
	R	G	B
Y	+0.299	+0.587	+0.114
C_B	-0.169	-0.331	±0.5
C_R	+0.5	-0.419	-0.081

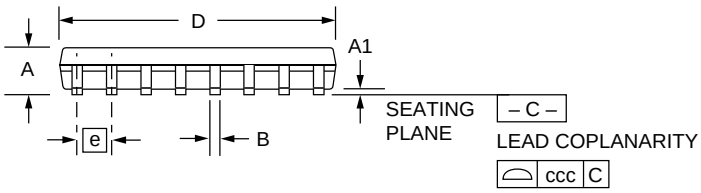
Mechanical Dimensions – 16-Lead SOIC

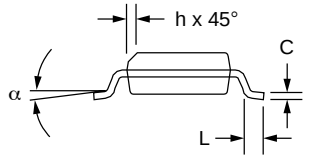
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.386	.394	9.80	10.00	2
E	.150	.158	3.81	4.00	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.80	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6702M	0° to 70°C	Commercial	16 Pin Narrow SOIC	RC6702M

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